UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,979	03/11/2004	Jeffery Steven Beck	MICR-161US	6873

68551 7590 11/01/2007

RatnerPrestia
P.O. BOX 980
VALLEY FORGE, PA 19482

EXAMINER	
NGUYEN, LUONG TRUNG	
ART UNIT	**PAPER NUMBER**
2622	

MAIL DATE	DELIVERY MODE
11/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/798,979	BECK ET AL.	
	Examiner	Art Unit	
	LUONG T. NGUYEN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12,14-16 and 18-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12,14-16 and 18-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-12, 14-16, 18-21 filed on 7/18/2007 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claims 1-5, 11-12, 14-16, 18-21 are objected to because of the following informalities:

Claim 1 (line 5), "include" should be changed to --include:--.

Claim 11 (line 3), claim 15 (line 4), claim 21 (line 2), "having" should be changed to --having:--.

Claim 15 (line 5), "output" should be changed to --output,--.

Claim 12 (lines 2-3), "the amplifier being of the video circuit a single ended common source amplifier" should be changed to --the amplifier includes a single ended common source amplifier--.

Claim 14 (lines 1-2), "wherein the sample and hold circuit" should be changed to --wherein the closed loop sample and hold circuit--.

Claims 2-5 are objected as being dependent on claim 1.

Claims 12, 14, 20-21 are objected as being dependent on claim 11.

Claim 16, 18-19 are objected as being dependent on claim 15.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 21 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Newly added claim 21 recites new limitation "the further capacitor coupled between the column input and the input of the amplifier when the capacitor of the video circuit is in the second mode and being coupled between the input and output of the further amplifier when the capacitor of the video circuit is in the first mode," there is no disclosure in the specification to support for this limitation.

It should be noted that the specification, pages 4-6 and Figure 2 discloses the reference amplifier 160 which reads on "reset circuit" as claimed in claim 21; amplifier 162 which reads on "further amplifier" as claimed in claim 21; capacitor C2 which reads on "further capacitor" as claimed in claim 21; the amplifier 142 which reads on "the amplifier" as claimed in claim 21, the amplifier 142 is included in video amplifier 140 which reads on "the video circuit." The specification, page 4, paragraphs [21] and [22] disclose that the video amplifier circuit 140 and reference amplifier circuit 160 operate in the same manner (i.e., the operations of circuits 140 and 160 is identical). This means that in a first mode, capacitor C1 (a capacitor) is coupled between column input and the input of the amplifier 142, and capacitor C2 (a further capacitor)

is coupled between column input and the input of the amplifier 162; and in a second mode, capacitor C1 is coupled between the input of the amplifier 142 and the output of the amplifier 142, and capacitor C2 (further capacitor) is coupled between the input of the amplifier 162 and the output of the amplifier 162. There is no disclosure to show that the further capacitor (capacitor C2) is coupled between the column input and the input of the amplifier (amplifier 142) when the capacitor (capacitor C1) of the video circuit is in the second mode and being coupled between the input and output of the further amplifier (amplifier 162) when the capacitor of the video circuit is in the first mode as newly added in newly added claim 21.

For the purpose of examination, this limitation of claim 21 will be interpreted as "the further capacitor coupled between the column input and the input of the further amplifier in a first mode and being coupled between the input and output of the further amplifier in a second mode," since the operation of circuits 140 and 160 is identical.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-12, 14-16, 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borg et al. (US 6,476,864) in view of Morse et al. (US 4,786,831).

Regarding claim 1, Borg et al. discloses an active pixel sensor array sampling system comprising:

at least one video circuit (amplifier 230, figure 3A, 4, column 6, lines 17-60) that generates a video voltage from each one of a group of pixels;

at least one reset circuit (amplifier 240 and transistor 330 with reset signal 118, figure 4, column 4, line 3 – column 8, line 12) that generates a reset voltage associated with each one of the pixels in the group of pixels;

wherein one or more of the video or reset circuits include:

an amplifier having an input and an output (amplifier 80 or 110, figure 4, column 7, lines 4- 45);

a column input (common column line 38, figure 4, column 7, lines 4- 45) having one of the video or reset voltage thereon;

a capacitor such that in a first mode the capacitor is coupled between the column input and the input of the amplifier (capacitor 78 is coupled between the column input 38 and the input of the amplifier 80, figure 4, column 7, lines 4-45).

Borg et al. fails to specifically disclose a capacitor such that in a second mode the capacitor is coupled between the input of the amplifier and the output of the amplifier. However, Morse et al. teaches an amplifier circuit 12, which comprises a coupling capacitor 14 and a capacitor reset switch 24; when the capacitor reset switch 24 is closed in a first time period, the capacitor 14 is coupled between the input of the amplifier 12 and the output 22 of the amplifier 12 (figure 3, column 2, line 53 – column 3, line 25), which corresponds to the second mode; when the capacitor reset switch 24 is opened in a second time period, the capacitor 14 is coupled

between the column input node 20 and the input of the amplifier 12 (figure 3, column 2, line 53 – column 3, line 25), which corresponds to the first mode. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Borg et al. by the teaching of Morse et al. in order to obtain an amplifier circuit for infrared detectors in which detector noise is reduced and detector responsivity uniformity is improved (column 2, lines 25-29).

Regarding claim 2, Borg et al. discloses wherein the amplifier includes a single ended common source amplifier (amplifier 80, figure 4, column 6, lines 39-60).

Regarding claim 3, Borg et al. discloses wherein the capacitor (capacitor 78 or 108, figure 4) holds the one of the video the reset voltage.

Regarding claim 4, Morse et al. discloses wherein the one or more of the video and reset circuits further include switches that place the capacitor across the input and the output of the amplifier (when switches 24, 16 are closed, the capacitor 14 is connected to the input and the output of the amplifier 12 figure 4, column 3, lines 5-33).

Regarding claim 5, Borg et al. discloses wherein the pixels are arranged in columns and rows (figure 3A), the at least one video circuit comprises a plurality of video amplifiers (amplifiers 230, figure 3A), each video amplifier being associated with a respective column of

pixels, and wherein the at least one reset circuit comprises a plurality of reset amplifiers (amplifier 240, figure 3A), each reset amplifier being associated with one of the video amplifiers.

Regarding claim 6, Borg et al. discloses an active pixel sensor array sampling system comprising:

a video circuit (amplifier 230, figure 3A, 4, column 6, lines 17-60) that generates a video voltage from each one of a group of pixels;

a reset circuit (amplifier 240 and transistor 330 with reset signal 118, figure 4, column 4, line 3 – column 8, line 12) associated with the video circuit that generates a reset voltage associated with each one of the pixels in the group of pixels;

wherein the video or reset circuits each include an amplifier having an input and an output (amplifier 80 or 110, figure 4, column 7, lines 4- 45), a column input (common column line 38, figure 4, column 7, lines 4- 45) having one of the video or reset voltage thereon, and a capacitor selectively coupled between the column input and the input of the amplifier (capacitor 78 is coupled between the column input 38 and the input of the amplifier 80, figure 4, column 7, lines 4-45).

Borg et al. fails to specifically disclose the capacitor is coupled between the input of the amplifier and the output of the amplifier. However, Morse et al. teaches an amplifier circuit 12, which comprises a coupling capacitor 14 and a capacitor reset switch 24; when the capacitor reset switch 24 is closed in a first time period, the capacitor 14 is coupled between the input of the amplifier 12 and the output 22 of the amplifier 12 (figure 3, column 2, line 53 – column 3, line 25); when the capacitor reset switch 24 is opened in a second time period, the capacitor 14 is

coupled between the column input node 20 and the input of the amplifier 12 (figure 3, column 2, line 53 – column 3, line 25). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Borg et al. by the teaching of Morse et al. in order to obtain an amplifier circuit for infrared detectors in which detector noise is reduced and detector responsivity uniformity is improved (column 2, lines 25-29).

Regarding claim 7, Borg et al. discloses wherein the amplifier of each of the video and reset circuits comprises a single ended common source amplifier (amplifier 80, figure 4, column 6, lines 39-60).

Regarding claim 8, Borg et al. discloses wherein the capacitors (capacitors 78,108, figure 4) of the video and reset circuits hold the video voltage and the reset voltage respectively.

Regarding claim 9, Morse et al. discloses the video and reset circuits include a plurality of switches such that the plurality of switches are configured to place a respectively capacitor across the input and the output of the associated amplifier (when switches 24, 16 are closed, the capacitor 14 is connected to the input and the output of the amplifier 12 figure 4, column 3, lines 5-33).

Regarding claim 10, Borg et al. discloses wherein the pixels are arranged in columns and rows and wherein the group of pixels is a column of pixels (group of pixels on each column 38, figure 3A).

Regarding claim 11, Borg et al. discloses a video amplifier (amplifier 230, figure 3A, 4, column 4, lines 15-45; column 6, lines 17-60) for use in sampling an active pixel sensor array (an active pixel sensor array 280, figure 3A, column 6, lines 17-60), the video amplifier comprising a video circuit having an amplifier with an input and an output (amplifier 80 or 110, figure 4, column 7, lines 4- 45), a column input (common column line 38, figure 4, column 7, lines 4- 45) having a video voltage thereon, and a capacitor such that in a first mode the capacitor coupled between the column input and the input of the amplifier (capacitor 78 is coupled between the column input 38 and the input of the amplifier 80, figure 4, column 7, lines 4-45).

Borg et al. fails to specifically disclose a capacitor such that in a second mode the capacitor is coupled between the input of the amplifier and the output of the amplifier. However, Morse et al. teaches an amplifier circuit 12, which comprises a coupling capacitor 14 and a capacitor reset switch 24; when the capacitor reset switch 24 is closed in a first time period, the capacitor 14 is coupled between the input of the amplifier 12 and the output 22 of the amplifier 12 (figure 3, column 2, line 53 – column 3, line 25), which corresponds to the second mode; when the capacitor reset switch 24 is opened in a second time period, the capacitor 14 is coupled between the column input node 20 and the input of the amplifier 12 (figure 3, column 2, line 53 – column 3, line 25), which corresponds to the first mode. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Borg et al. by the teaching of Morse et al. in order to obtain an amplifier circuit for infrared detectors in which detector noise is reduced and detector responsivity uniformity is improved (column 2, lines 25-29).

Regarding claim 12, Borg et al. discloses wherein the video circuit includes closed loop sample and hold circuit (figure 4, column 4, lines 20-25), the amplifier being of the video circuit a single ended common source amplifier (amplifier 80, figure 4, column 6, lines 39-60).

Regarding claim 14, Morse et al. discloses wherein the sample and hold circuit includes a plurality of switches configured to place the capacitor across the input and output of the amplifier of the video circuit (when switches 24, 16 are closed, the capacitor 14 is connected to the input and the output of the amplifier 12; figure 4, column 3, lines 5-33).

Regarding claim 15, Borg et al. discloses an integrated circuit including a video amplifier (amplifier 230, figure 3A, 4, column 4, lines 15-45); column 6, lines 17-60) for use in sampling an active pixel sensor array (an active pixel sensor array 280, figure 3A, column 6, lines 17-60),

a video and reset circuit having an amplifier with an input and an output (amplifier 80 or 110, figure 4, column 7, lines 4- 45), a column input (common column line 38, figure 4, column 7, lines 4- 45) having a video voltage thereon, and a capacitor for holding the video voltage such that the capacitor is selectively switched between the column input and the input of the amplifier (capacitor 78 is coupled between the column input 38 and the input of the amplifier 80, figure 4, column 7, lines 4-45).

Borg et al. fails to specifically disclose the capacitor is coupled between the input of the amplifier and the output of the amplifier to transfer the video voltage. However, Morse et al. teaches an amplifier circuit 12, which comprises a coupling capacitor 14 and a capacitor reset switch 24; when the capacitor reset switch 24 is closed in a first time period, the capacitor 14 is

coupled between the input of the amplifier 12 and the output 22 of the amplifier 12 (figure 3, column 2, line 53 – column 3, line 25); when the capacitor reset switch 24 is opened in a second time period, the capacitor 14 is coupled between the column input node 20 and the input of the amplifier 12 (figure 3, column 2, line 53 – column 3, line 25). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Borg et al. by the teaching of Morse et al. in order to obtain an amplifier circuit for infrared detectors in which detector noise is reduced and detector responsivity uniformity is improved (column 2, lines 25-29).

Regarding claim 16, Borg et al. discloses wherein the amplifier of the video and reset circuit comprises a single ended common source amplifier (amplifier 80, figure 4, column 6, lines 39-60).

Regarding claim 18, Morse et al. discloses wherein the video and reset circuit includes a plurality of switches configured to place the capacitor either across the input and output of the amplifier of the video and reset circuit in a first mode or to place the capacitor across the column input and the input of the amplifier of the video and reset circuit in a second mode (when switches 24, 16 are closed, the capacitor 14 is connected to the input and the output of the amplifier 12 which corresponds to the first mode; when the switches 24, 16 are opened, the capacitor 14 is coupled between the input node 20 and the input of the amplifier 12 which corresponds to the second mode; figure 4, column 3, lines 5-33).

Regarding claim 19, Borg et al. discloses wherein the integrated circuit is a CMOS integrated circuit (active pixel sensor array 280, figure 3A, column 1, lines 43-54).

Regarding claim 20, Borg et al. discloses wherein the video circuit includes a video sample and hold circuit (figure 4, column 4, lines 20-25) and the video sample and hold circuit includes a single capacitor (capacitor 78, figure 4).

Regarding claim 21, Borg et al. discloses a reset circuit having a further amplifier (amplifier 110, figure 4, column 7, lines 4-45) with a further input and a further output; and further capacitor (capacitor 108 is coupled between the column input 102 and the input of the amplifier 110, figure 4) coupled between the column input and the input of the further amplifier (amplifier 110, figure 4) in a first mode.

Borg et al. does not disclose the further capacitor is coupled between the input of the amplifier and the output of the amplifier in a second mode. However, Morse et al. teaches an amplifier circuit 12, which comprises a coupling capacitor 14 and a capacitor reset switch 24; when the capacitor reset switch 24 is closed in a first time period, the capacitor 14 is coupled between the input of the amplifier 12 and the output 22 of the amplifier 12 (figure 3, column 2, line 53 – column 3, line 25), which corresponds to the second mode; when the capacitor reset switch 24 is opened in a second time period, the capacitor 14 is coupled between the column input node 20 and the input of the amplifier 12 (figure 3, column 2, line 53 – column 3, line 25), which corresponds to the first mode.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571) 272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID L. OMETZ can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LN
10/29/07

Luonghuran Nguyen

LUONG T. NGUYEN
PATENT EXAMINER